In the Drawings

"Replacement Sheets" are attached which include a clean version of amended Figures 1, 2A and 2B. The attached sheets replace the original sheets including Figures 1, 2A and 2B. Figures 1, 2A and 2B have been amended to include the legend –Prior Art–, as requested in the Office Action. Figure 5 has been canceled, as discussed below.

REMARKS

In response to the Office Action mailed April 19, 2005, Applicant respectfully requests reconsideration. Claims 1-8 were previously pending in this application. Claim 1 has been amended. New claims 9-29 have been added to more fully define Applicant's contribution to the art. As a result, claims 1-29 are pending for examination with claims 1 and 9 being independent claims. No new matter has been added.

Objections to the Specification

The Office Action objected to the Specification because Figure 5 was not described in the Specification. It is respectfully requested that Figure 5 be cancelled from the present application.

Accordingly, withdrawal of this objection is respectfully requested.

Objections to the Drawings

The Office Action objected to the drawings because Figures 1, 2A and 2B did not include the legend "prior art." Figures 1, 2A and 2B have been amended to include the legend "prior art."

Accordingly, withdrawal of this objection is respectfully requested.

Information Disclosure Statement

As requested in the Office Action, copies of the two non-patent references cited on the IDS filed November 19, 2003 are enclosed herewith.

Rejections Under 35 U.S.C. §102

The Office Action rejected claims 1-8 under 35 U.S.C. §102(b) as being anticipated by Iwahashi (U.S. Patent No. 5,953,274). Applicant respectfully traverses this rejection.

Iwahashi is directed to a semiconductor memory device. Each memory cell includes one MOS transistor. More than one bit may be stored per memory cell by using an appropriately doped and sized channel region of the MOS transistor (abstract).

FIG. 16 illustrates the architecture of the semiconductor memory. The memory includes multiple bit lines (e.g., BL1 and BL2) that are each coupled to a column of memory cells. Bit

line BL1 may be selected by applying a signal to transistor 72_1. Bit line BL2 may be selected by applying a signal to transistor 72_2.

A column decoder 73 is used to apply a signal to the appropriate column selection transistor (e.g., 72_1 or 72_2) for the column of memory cells to be selected. Thus, each column is selected by a corresponding activation line that is coupled to the gate of the respective column selection transistor (e.g., 72_1 or 72_2). Each activation line from column decoder 73 is only coupled to a single column of the semiconductor memory.

By contrast, claim 1, as amended, recites, *inter alia*, that the columns are arranged in groups of two adjacent columns, each column in a group being selectable with respect to the other column in the group by an activation line, wherein each column in a group is connected by one end to another activation line that selects the other column in the group. Iwahashi does not teach or suggest that each column in a group is connected by one end to another activation line that selects the other column in the group. Therefore, claim 1 patentably distinguishes over Iwahashi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-8 depend from claim 1 and are therefore patentable for at least the same reasons.

New Claims

New claim 9 relates to a memory circuit that includes a first column of memory cells coupled to a first bit line and a second column of memory cells coupled to a second bit line. A first block select line provides a first signal to select the first column. The first block select line is coupled to the first column and the second column. A second block select line provides a second signal that is complementary to the first signal. The second block select line is coupled to the first column and the second column. Claim 9 is patentable over Iwahashi because Iwahashi does not teach or suggest a second block select line that provides a second signal that is complementary to the first signal, the block select line being coupled to the first column and the second column.

Claims 10-29 depend from claim 9 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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By: _____

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